REMARKS

By this Amendment, claims 2, 3, 8-11, 13 and 18-21 are amended and claim 1 is canceled. Accordingly, claims 2-3, 5-13 and 15-21 are pending in this application. Reconsideration of the application is respectfully solicited.

Support for the claim amendments may be found in the specification, for example, on page 8, lines 6-8, and page 9, lines 15-22, and in Fig. 5.

Applicants submit that neither U.S. Patent No. 5,301,328 to Benson nor U.S. Patent No. 6,035,120 to Ravichandran discloses or suggests "a controller that divides the source code into first source code blocks based on branches and loops in the source code, and divides the first source code blocks into second source code blocks, a largest number of source registers required in each second source code block being less than or equal to a number of target registers that correspond to the source registers, and converts each of the second source code blocks directly into a corresponding target code block," as recited in claims 11 and 21 and that therefore, claims 11 and 21 are patentable over the applied references.

Although Benson arguably divides the source code into first source code blocks based on branches and loops, Benson does not divide the first source code blocks into second source code blocks, a largest number of source registers required in each second source block being less than or equal to a number of target registers that correspond to the source register. Also, Benson does not convert each of the second source code blocks directly into a corresponding target code block, as Benson translates the source code into an internal representation which is independent of the target machine architecture (see column 9, lines 8-13).

Although Ravichandran does arguably convert source codes into target codes, Ravichandran does not divide the source code into first or second source code blocks. Instead, Ravichandran "maps each instruction associated with the source processor to one or more valid instructions associated with the target processor" (see column 5, lines 63-65).

By dividing the first source code blocks into second source code block, a largest number of source registers required in each source code block being less than or equal to a number of target registers that correspond to the source registers, the translation from source code to target code can be performed more simply and quickly.

Furthermore, neither Benson nor Ravichandran discloses or suggests "a source register map having a number of storage locations based on a number of instruction cycles required to update a source register." By including these storage locations in the source register map, the code translation device can accommodate delays in the update times of various source registers.

Claim 2 is amended to depend from claim 21. Claims 3, 8-10, 13 and 18-20 are amended to be consistent with the amendments made to claims 11 and 21.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 2-3, 5-13 and 15-21 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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